REMARKS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed on September 3, 1999.

The specification is objected to for minor informalities. The title of the invention is objected to for being non-descriptive.

Claims 1-5, 8, 10-12, and 14-17 stand rejected under 35 U.S.C. §102(b) as being anticipated by "Memory Systems Design and Applications", edited by Dave Bursky, pp. 213-220 ("Bursky").

Claims 6, 7, 9, and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Bursky.

Claims 1-17 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09/023,170 and claims 1-14 of copending Application No. 09/023,172.

Claims 1-17 are pending. Claims 1-3, 5-9, and 14-17 have been amended. Applicant respectfully submits that no new matter has been introduced by the amendments made herein.

The Examiner has objected to the specification on page 2 for having missing serial numbers. Accordingly, the specification has been amended to provide the appropriate serial numbers.

The Examiner has objected to the title of the invention as being non-descriptive. Accordingly, the title of the invention has been amended. Applicant

respectfully submits that the amended title is clearly indicative of the invention to which the claims are directed.

The Examiner has rejected claims 1-5, 8, 10-12, and 14-17 under 35 U.S.C. §102(b) as being anticipated by Bursky. In particular, the Examiner states:

> Regarding claims 1, 2, 8, and 15-17 on page 217 Bursky teaches in the photo caption that "System costs plummet when function duplication is designed out. While most minis duplicate read/write and control electronics for each board of memory DIPs, Interdata makes one read/write/control set serve more memory, by using eight little 'daughter boards.' The packaging also simplifies reconfiguration and speeds up field repair" (emphasis added).
>
> Furthermore, on page 219, third column, he writes that "The PC-board economy is possible through the use of 'daughter boards," strips that are 8 in. long, 1 in. wide and plug into the 15x15 in. memory board itself. Not only does this mean that 256 k-bytes can be packed on the board instead of 32 or 64 k-bytes, it also means that function duplication is cut back. As a result, the read/write control logic that would have been duplicated on a series of 64 k-byte boards appears just once on the 15x15 in. motherboard, serving all 256 k-bytes. Larry MacPherson, Interdata product manager for the Series Sixteen, points out that this unusual modularity makes it easy to add and subtract memory in the field, and slashes the cost of incremental memory increases" (emphasis added).
>
> Bursky's focus in the passages above is toward the daughter card system of Interdata. However, the underlined passage above teach that it was known to use memory controllers on individual memory modules, each of which contained a plurality of memory device as claimed. In fact, such a design appears to have been the norm. The passages above describe a new (for the time) method of reducing the duplication of the memory controllers by removing them from the memory modules and using a single controller on the motherboard for all memory modules (daughter cards). This is the standard today, and is the admitted prior art of the instant application. However, in 1980 and before, it was common to include the memory controller on each memory module as taught above.
>
> Bursky does not explicitly teach that the memory module controller reformats the transactions it receives before passing them on to the plurality of memory devices, however such

reformatting is inherent in the devices described by Bursky since memory devices required different format signals than memory module controllers. Bursky does not characterize the memory controllers of the memory modules other than to call them read/write/control logic, which meets the broad claim language of handling requests (reads or writes) and controlling transactions.

Applicant respectfully submits that claim 1, as amended, is not anticipated by Bursky. Claim 1 includes the limitations of:

> A memory module, comprising:
> a plurality of memory devices; and
> a memory module controller configured to receive a first memory transaction in a first format from a first memory bus, and to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

(Claim 1)(emphasis added).

In contrast to claim 1, Bursky fails to disclose a memory module having a memory module controller configured to receive a first memory transaction in a fist format from a first memory bus and to convert the first memory transaction into a second memory transaction in a second format. In further contrast to claim 1, Bursky fails to disclose or suggest the second format of the second memory transaction being different from the first format of the first memory transaction.

Bursky relates generally to providing reliability to memory devices by using error correction capability. See Bursky pp. 216-220. The Examiner, however, relies on the following sections of Bursky to support the §102(b) rejection.

> System costs plummet when function duplication is designed out. While most minis duplicate read/write and control electronics

> for each board of memory DIPS, Interdata makes one read/write/control set serve more memory, by using eight little "daughter boards." This packaging also simplifies reconfiguration and speeds up field repair.

(Bursky p.217, photo caption text).

> The PC-board economy is possible through the use of "daughter boards," strips that are 9-in.long, 1-in. wide and plug into the 15x15-in. memory board itself. Not only does this mean that 256 kbytes can be packed on the board instead of 32 or 64 kbytes, it also means that function duplication is cut back.
>
> As a result, the read/write control logic that would have been duplicated on a series of 64-kbyte boards appears just once on the 15x15-in. motherboard, serving all 256 kbytes.

(Bursky p.219).

Applicant respectfully submits that the above sections of Bursky do not teach or suggest converting a first memory transaction in a first format into a second memory transaction in a second format by a memory module controller for a plurality of memory devices. The Examiner asserts that the read/write/control logic of Bursky teach inherently reformatting of transactions. It is respectfully submitted that this assertion is unsupported. The read/write/control logic taught by Bursky is used to perform read and write transactions for memory devices. Furthermore, Bursky provides no teaching of converting a memory transaction in one format into another format.

For the above reasons, applicant respectfully submits that claim 1 is not anticipated by Bursky, and is in condition of allowance. Given that claims 2-16 depend directly or indirectly on claim 1, applicant respectfully submits that claims 2-16 are not anticipated by Bursky, and are in condition of allowance for the same reasons as claim 1.

Applicant respectfully submits that claim 17, as amended, is not anticipated by Bursky. Claim 17 includes the limitations of:

> A memory module, comprising:
> a plurality of memory devices; and
> a memory module controller coupled to the plurality of memory devices, the memory module controller being configured to receive a first memory transaction in a first format from a memory bus, and to convert the first memory transaction into a second memory transaction in a second format, and to provide the second memory transaction in the second format to at least one of the plurality of memory devices.

(Claim 17)(emphasis added).

In contrast to claim 17, Bursky fails to disclose or suggest a memory module having a memory module controller configured to receive a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format and to provide the second transaction in the second format to at least one of the plurality of memory devices.

As stated previously, nowhere in Bursky does it teach converting memory transactions in one format to another. For the above reasons, claim 17 is not anticipated by Bursky, and is in condition of allowance.

The Examiner has rejected claims 6, 7, 9, and 13 under 35 U.S.C. §103(a) as being unpatentable over Bursky. Given that claims 6, 7, 9, and 13 depend directly or indirectly on claim 1, applicant respectfully submits claims 6, 7, 9, and 13 are not rendered unpatentable over Bursky for the same reasons claim 1 is not anticipated by Bursky.

The Examiner has provisionally rejected claims 1-17 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of co-pending Application No. 09/023,170 and claims 1-14 of co-pending application 09/023,172.

Upon a condition of allowance of one or more claims, applicant will submit a terminal disclaimer.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the rejections and objections set forth in the Office Action mailed September 3, 1999 have been overcome. Accordingly, applicant respectfully request that claims 1-17, as amended, be found in condition of allowance.

If a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Mike Kim at (408) 720-8300 x345.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

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